

INT2769 Catalog

1





INT2769 Description:

INT2769 is a USB-powered Universal GPS/Galileo/Glonass Receiver that uses MAX2769B to receive the High Frequency signals from Active/Passive antennas. A microcontroller connected to USB port sets the registers of the MAX2769 to prepare it to work in the desired mode. The data for setting the registers are received from a PC through USB port.

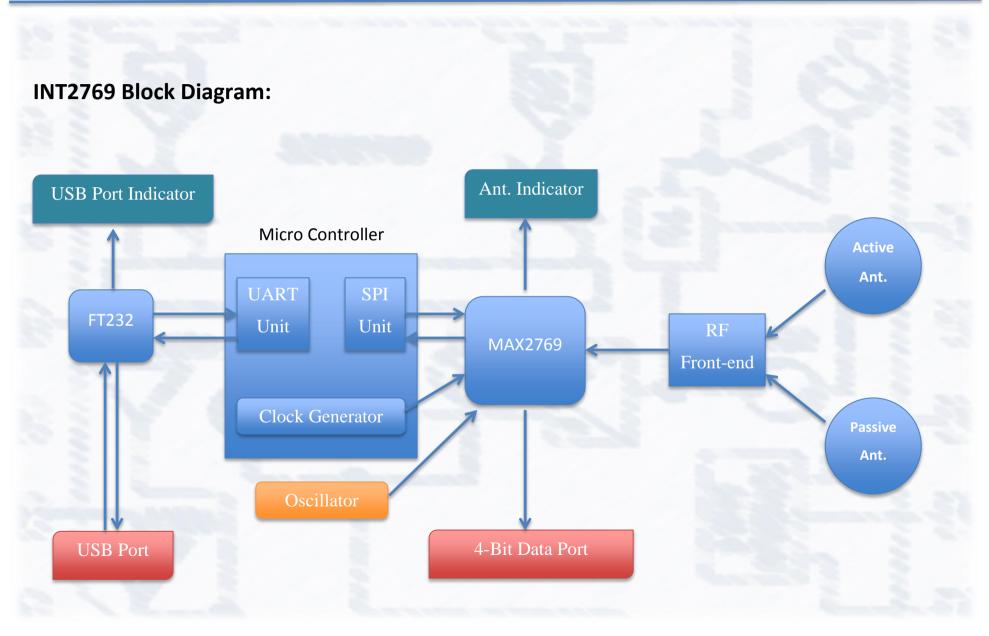
A user-friendly GUI is designed to make the user able to choose different values for registers through software. The I and Q data received from GPS/Galileo/Glonass satellites are converted to digital signals using internal ADC and conducted to the 4-Bit Data Port. The 4-Bit Data Port can be connected directly to a FPGA, DSP or Microcontroller for data analysis.

This module also conjunctly works with INT9121 module, which collects the data from INT2769 to transfer them to a PC through a high speed USB port.

INT2769 Specification:

- Receiving signals in a frequency range from 1550MHz to 1610MHz (GPS/Galileo/Glonass Bands)
- Compatible with Active and Passive antennas (SMA connector)
- Using MAX2769B as the front-end receiver
- Using Microcontroller for setting the registers of the MAX2769B
- Using the USB port for communication to the software
- USB powered
- LED indicators for Power, Active antenna and USB communication
- Data output is compatible with the FPGAs, DSPs and microcontrollers
- Fully compatible with INT9121 Module
- One year warranty







INT2769 GUI Screenshot:

	IF filter center BW		Current for XTAL osc			ILNA1 current:		
port setting	2.5MHz	•	buffer normal curr	•		4		
Chip enable	Mixer pole		IF filter gain			A2 currer	A2 current	
Idle	36MHz	•	reduce the filter g	-		•		
PWRSAV EN	LNA mode selection		Charge-pump test	t		iLO buffer curre		ent
Clk Buffer En Filter HiP En	Gated mode	•	normal operation	•		4		
mixer enable	AGC Mode		IQEN			Mixer current		nt
ANT Bias EN	Independent I&Q	•	I & Q enable	•		4		
LO buffer EN FSLOW EN	Output data format		Filter order					
HILOAD EN	Sign & Mag	•	5th-order Butterw	•				
ADC EN	Number bits of ADC		Polyphase filter				NDIV	
DRV EN FOFST EN	2 BIT	•	lowpass filter	•				
FILTEN	Output Level						FDIV	
PGALEN	CMOS logic	•						
PGAQ EN STRM EN	Number of bits streamed					5	Set Gains	
STRM start	IMSB, ILSB	•						
STRM stop	Clock output divider ratio						Set Freq	
STAMP EN	XTAL	•						